

FIG. 1

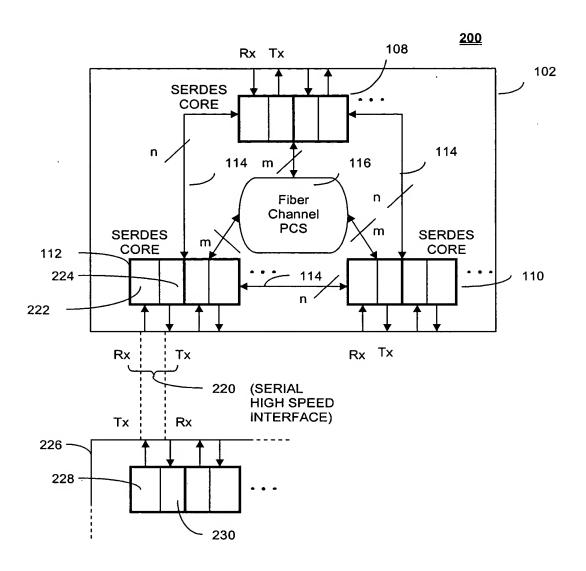


FIG. 2

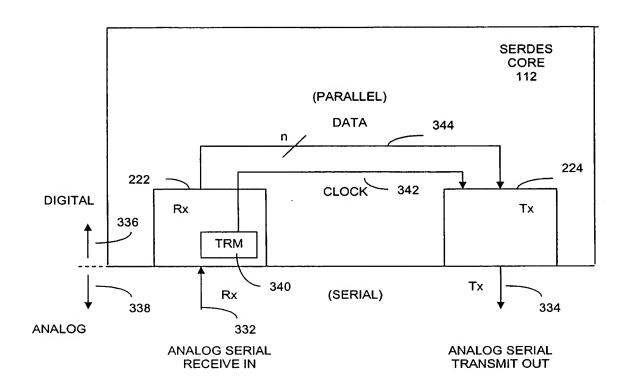


FIG. 3

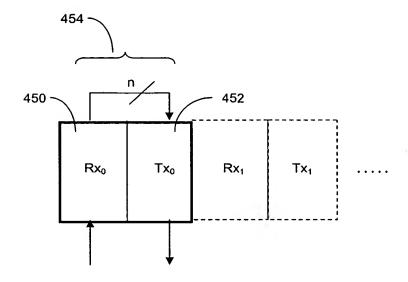
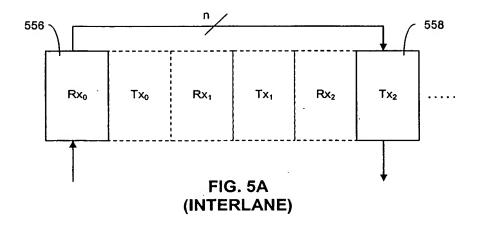


FIG. 4 (INTRALANE)



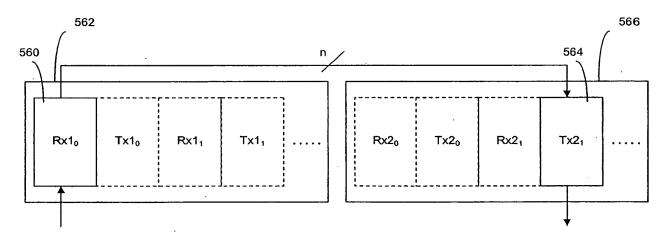
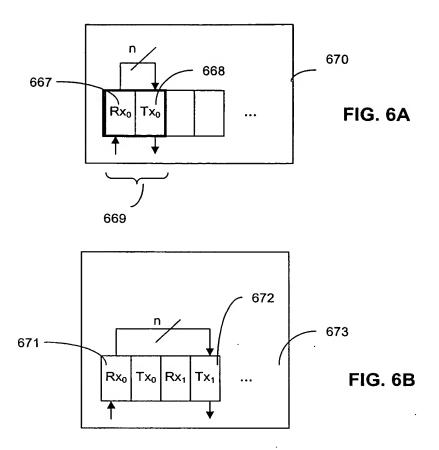


FIG. 5B (INTERLANE / INTERCORE)



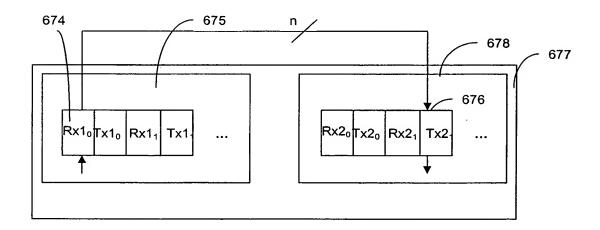


FIG. 6C

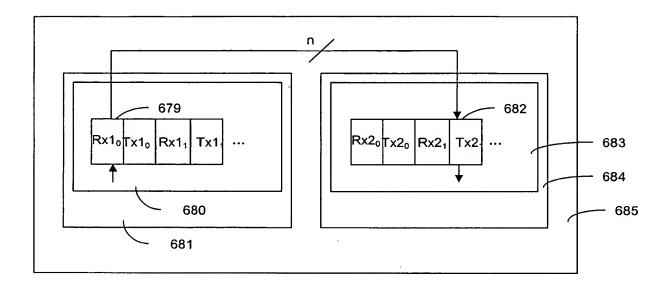


FIG. 6D

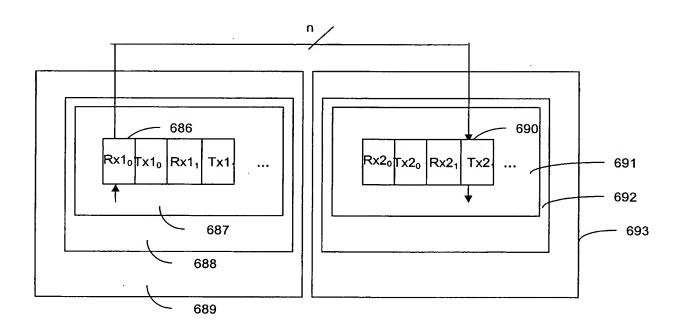
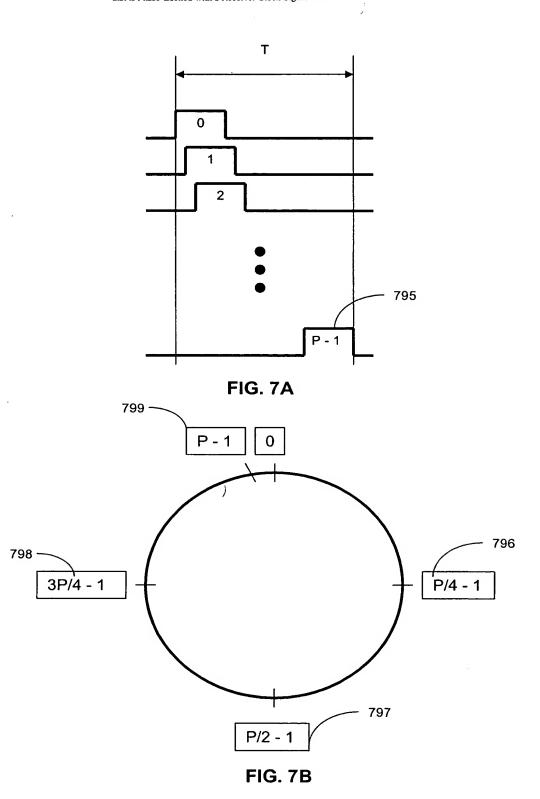


FIG. 6E



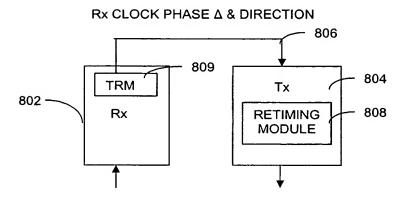


FIG. 8

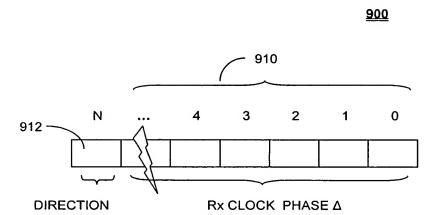


FIG. 9

Rx PREVIOUS CLOCK PHASE & Rx CURRENT CLOCK PHASE

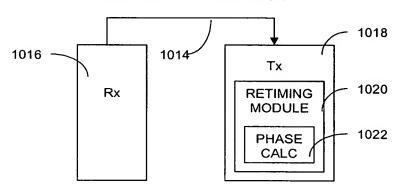


FIG. 10

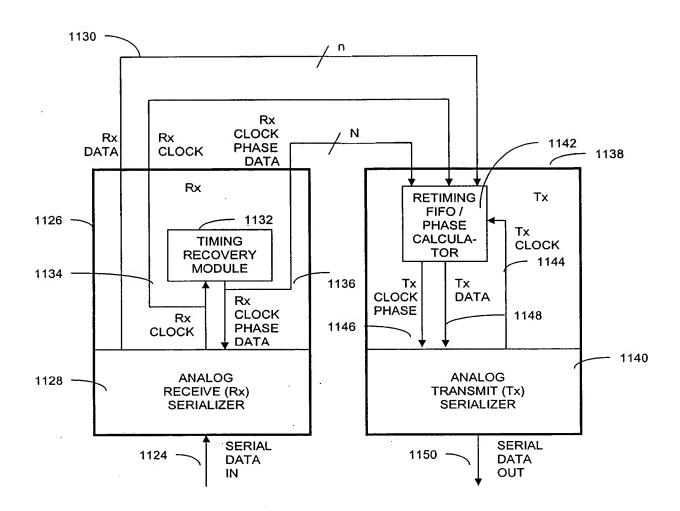


FIG. 11

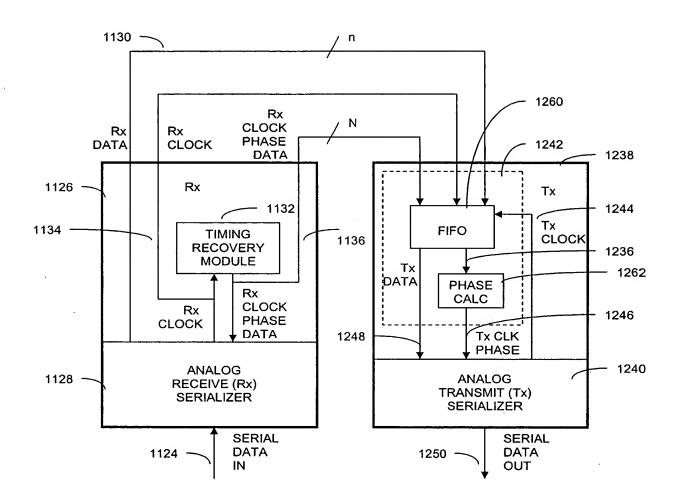


FIG. 12

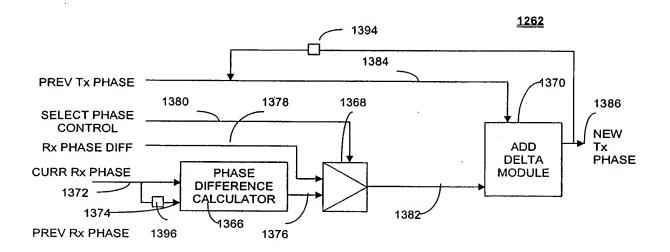


FIG. 13A

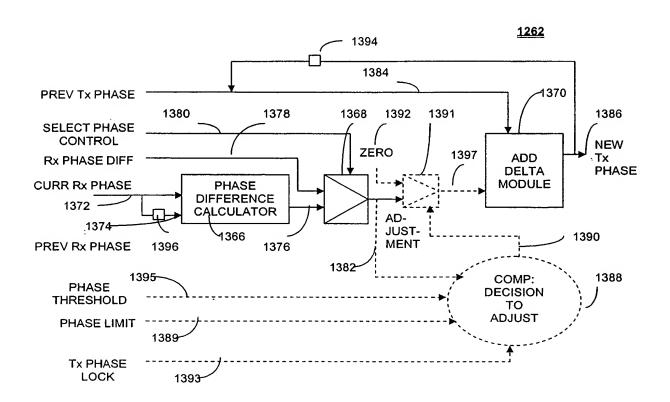


FIG. 13B

<u>1388</u>

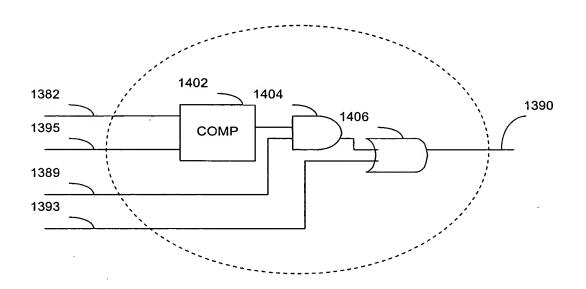


FIG. 14

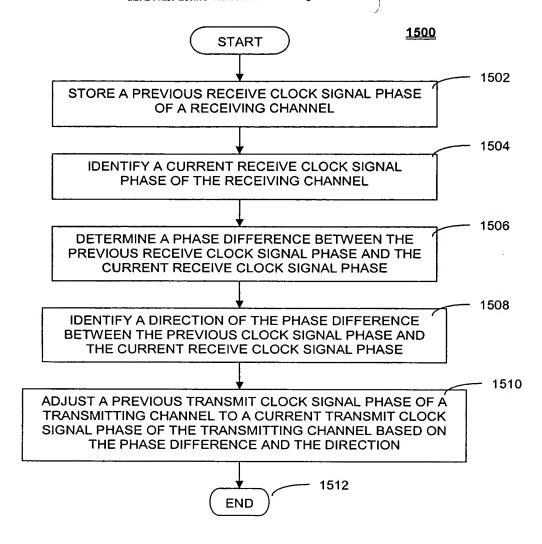


FIG. 15



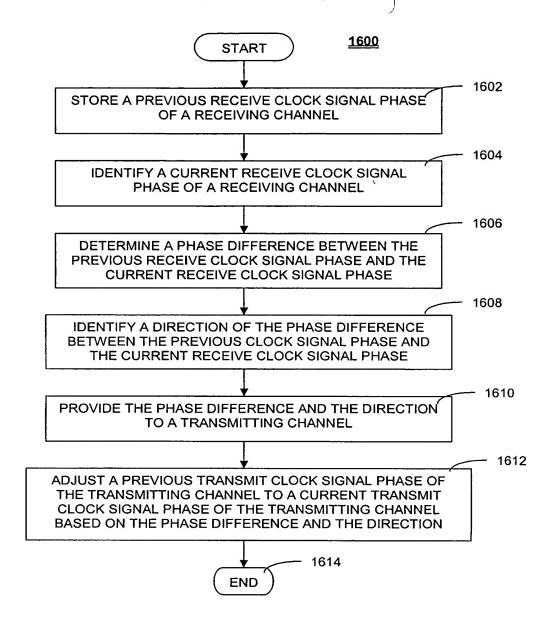


FIG. 16

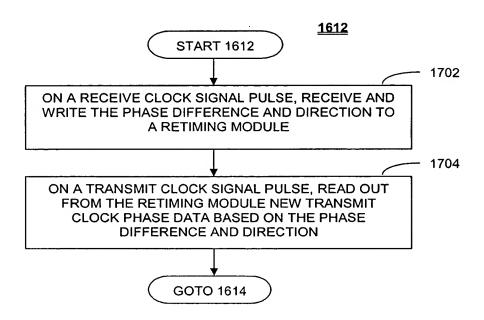


FIG. 17



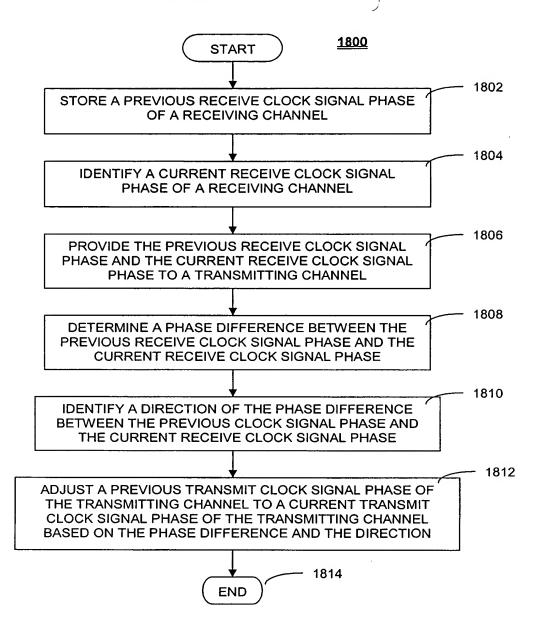


FIG. 18

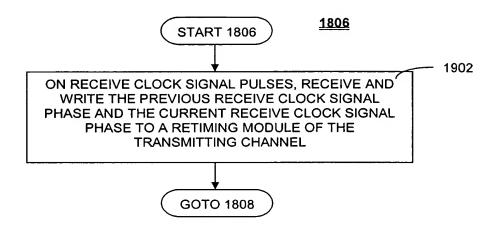


FIG. 19

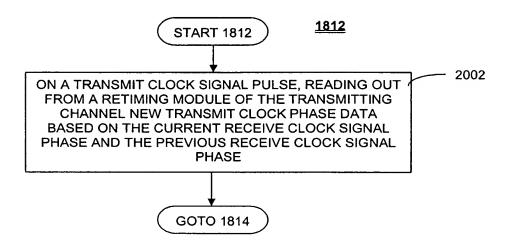


FIG. 20

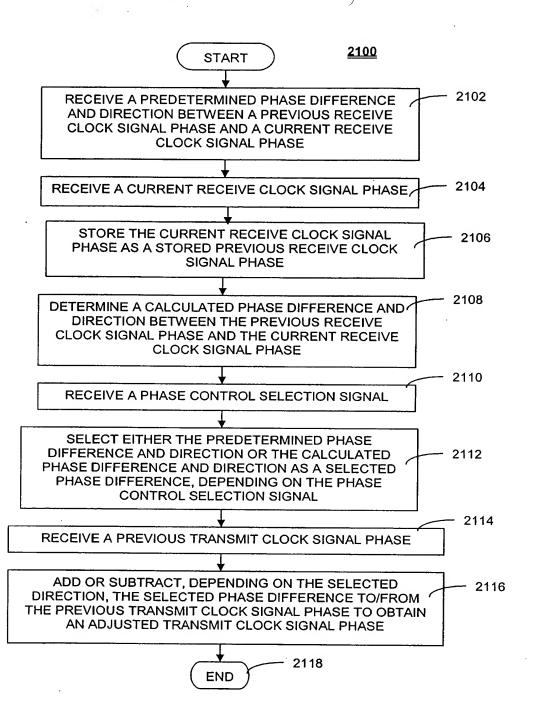


FIG. 21

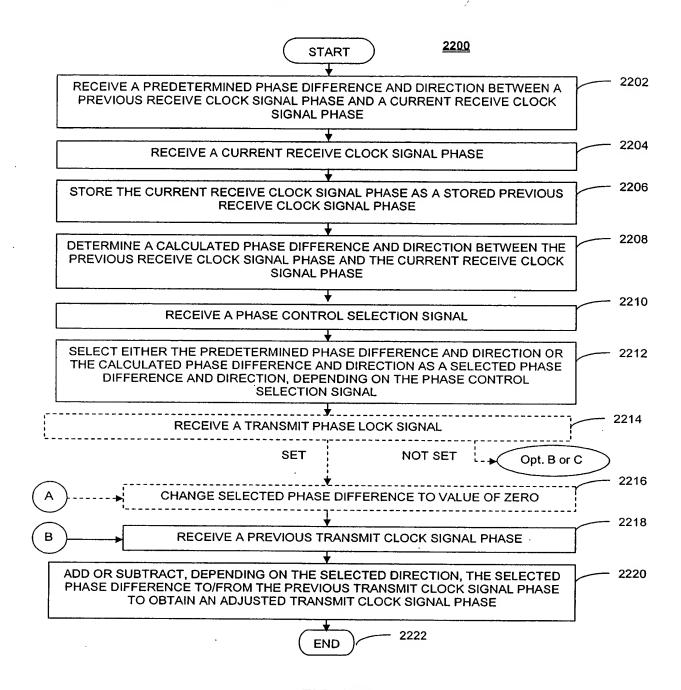


FIG. 22A

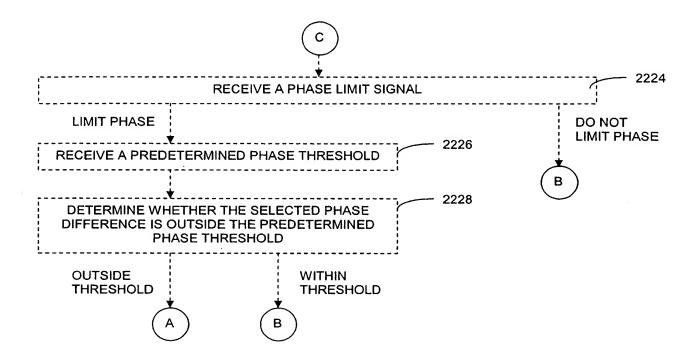


FIG. 22B



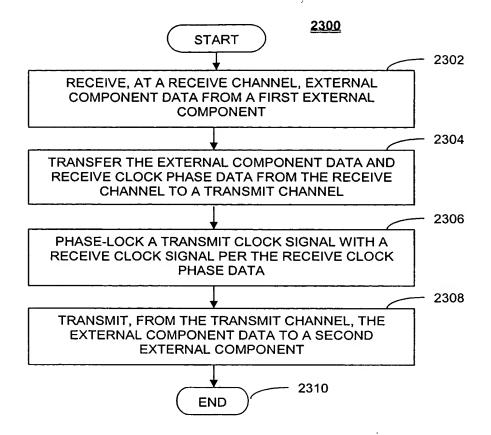


FIG. 23